

Amendments to the Claims:

Cancel claims 1-13, without prejudice.

The following listing of claims will replace all prior versions and listings of claims in the application:

1.-13. (canceled)

14. (withdrawn) A method for producing a light-emitting semiconductor component, comprising the steps of:

- (a) epitaxially depositing a light-emitting semiconductor layer (2) on a growth substrate (1),
- (b) providing the semiconductor layer (2) with a metallic contact layer (3),
- (c) producing an adhesion and wetting layer (6) at least above the metallic contact layer (3),
- (d) applying, producing or depositing a mechanically stable carrier substrate (7) onto the adhesion and wetting layer (6),
- (e) separating the semiconductor layer (2) from the growth substrate (1),
- (f) etching of mesa trenches (10) for the definition of individual chips between the mesa trenches (10), the mesa trenches (10) at least extending through the entire semiconductor layer (2) and the entire contact layer (3),
- (g) applying an electrical contact (8) on the semiconductor layer (2), and
- (h) singulating the chips by separation along the mesa trenches (10).

15. (previously presented) A method for producing a light-emitting semiconductor component, which has the following method steps:

(a) epitaxially depositing a light-emitting semiconductor layer (2) on a growth substrate (1),

(b) providing the semiconductor layer (2) with a metallic contact layer (3),

(ba) etching of mesa trenches (10) for the definition of individual chips between the mesa trenches (10), the mesa trenches (10) at least extending through the entire semiconductor layer (2) and the entire contact layer (3),

(c) producing an adhesion and wetting layer (6) at least above the metallic contact layer (3),

(d) applying, producing or depositing a mechanically stable carrier substrate (7) onto the adhesion and wetting layer (6),

(e) separating the semiconductor layer (2) from the growth substrate (1),

(g) applying an electrical contact (8) on the semiconductor layer (2), and

(h) singulating the chips by separation along the mesa trenches (10).

16. (currently amended) The method as claimed in claim [[14]] 15, in which, after method step (b) a reflection layer (4) is applied on the contact layer (3) or integrated in the contact layer (3).

17. (original) The method as claimed in claim 16, in which a diffusion barrier (5) is applied on the reflection layer (4).

18. (currently amended) The method as claimed in claim ~~[[14]]~~ 15, in which the contact layer in accordance with method step (b), the reflection layer (4), the barrier layer (5), the wetting layer (6) in accordance with method step (c) and/or the contact (8) in accordance with method step (g) are applied by means of sputtering or vapor deposition.

19. (currently amended) The method as claimed in claim ~~[[14]]~~ 15, in which a selectively dissolvable material is used for the growth substrate (1), and the separation of the semiconductor layer (2) from the growth substrate (1) in accordance with method step (e) is effected by selective etching of the growth substrate (1).

20. (currently amended) The method as claimed in claim ~~[[14]]~~ 15, in which prior to method step (a), a sacrificial layer (100) comprising a selectively dissolvable material is applied to the growth substrate, so that method step (a) takes place on said sacrificial layer (100), and the separation of the semiconductor layer (2) from the growth substrate (1) in accordance with method step (e) is effected by selective etching of the sacrificial layer (100).

21. (currently amended) The method as claimed in claim ~~[[14]]~~ 15, in which an already laminated substrate is used as the growth substrate (1), the laminated substrate having an adhesion layer (101) with suitable desired breaking locations (102) at which the growth substrate (1) is separated from the semiconductor layer (2) in a targeted manner during method step (e).

22. (currently amended) The method as claimed in claim ~~[[14]]~~ 15, in which the separation of the semiconductor layer (2) from the growth substrate (1) in accordance with method step (e) is effected by means of a laser lift-off method by using a laser to decompose the semiconductor layer (2) at the interface with the growth substrate (1).

23. (currently amended) The method as claimed in claim ~~[[14]]~~ 15, in which the mechanically stable carrier substrate (7) is deposited by means of a sputtering method, a CVD method, a galvanic method or electroless plating.

24. (currently amended) The method as claimed in claim ~~[[14]]~~ 15, in which, after method step (d), an additional auxiliary substrate (12) is applied to the carrier substrate (7).

25. (original) The method as claimed in claim 24, in which the additional auxiliary substrate (12) is fixed onto the carrier substrate (7) by means of an adhesive-bonding method or soldering.

26. (previously presented) The method as claimed in claim 24, in which a solder layer (11) required for soldering and/or the auxiliary substrate (12) are/is applied by means of sputtering, vapor deposition or galvanically.

27. (currently amended) The method as claimed in claim ~~[[14]]~~ 15, in which the carrier substrate (7) comprises a layer sequence, the layers of which are coordinated with one another in terms of thickness such that the layer having the largest modulus of elasticity (21) is

the thinnest and the layer having the smallest modulus of elasticity (20) is the thickest.

28. (currently amended) The method as claimed in claim [[14]] 15, in which the total thickness of the carrier substrate (7) and, if appropriate, of the auxiliary substrate (12) and of the solder or adhesive-bonding layer (11) does not exceed 15 micrometers.

29. (currently amended) The method as claimed in claim [[14]] 15, in which, after method step (g), a passivation layer (9) is applied at least partly over the semiconductor layer (2).

30. (currently amended) The method as claimed in claim [[14]] 15, in which, after method step (g), three-dimensional structures for optimizing the coupling-out of light are applied to the semiconductor layer (2) and/or, if present, to the passivation layer (9).

31. (original) The method as claimed in claim 30, in which the three-dimensional structures for optimizing the coupling-out of light are formed in pyramidal fashion with at least three visible areas per pyramid on the semiconductor layer (2) and/or the passivation layer (9) or in conical fashion on the semiconductor layer (2) and/or the passivation layer (9).

32. (previously presented) The method as claimed in claim 30, in which the three-dimensional structures for optimizing the coupling-out of light are produced by means of wet-chemical or dry etching.

33. (previously presented) The method as claimed in claim 15, in which, after method

step b), a passivation layer (9) is applied at least partly over the semiconductor layer (2), the contact layer (3) and, if present, also over the reflection layer (4) and the diffusion barrier (5).

34. (currently amended) The method as claimed in claim [[14]] 15, in which the chips are singulated by sawing or laser cutting in accordance with method step (h).

35. (previously presented) The method as claimed in claim 15, in which, after method step (c), separating ridges (13) are applied in the mesa trenches (10) on the wetting layer (6) in such a way that the separating ridges (13) completely fill the mesa trenches (10) over the entire length and project above the intervening surface of the wetting layer (6).

36. (original) The method as claimed in claim 35, in which the separating ridges (13) are applied with a height of at least 10 micrometers above the trench bottom.

37. (previously presented) The method as claimed in claim 35, in which a photoresist is used as material for the separating ridges (13).

38. (previously presented) The method as claimed in claim 35, in which the separating ridges are applied by means of photolithography or the LIGA method.

39. (previously presented) The method as claimed in claim 35, in which the separating ridges (13) are formed in such a way that they have a tip in cross section.

40. (previously presented) The method as claimed in claim 35, in which method step (d) takes place only in the spaces between the separating ridges (13) and the carrier substrate material is applied up to the height of the separating ridges (13).

41. (previously presented) The method as claimed in claim 35, in which method step (d) takes place only in the spaces between the separating ridges (13) and the carrier substrate material is applied beyond the height of the separating ridges (13).

42. (original) The method as claimed in claim 41, in which, after method step (g), the material of the separating ridges (13) is selectively removed.

43. (original) The method as claimed in claim 42, in which the material of the separating ridges (13) is dissolved by means of a solvent.

44. (previously presented) The method as claimed in claim 41, in which method step (h) is carried out by means of a shear process.

45. (previously presented) The method as claimed in claim 41, in which, during method step (h), the chips are singulated in strips (17) and are then mounted directly away from said strips (17) by means of a separating and bonding tool (18).

46. (original) The method as claimed in claim 40, in which

prior to method step (e), the material of the separating ridges (13) is selectively removed,

carrier substrate islands (71) arising,

the entire structure above the growth substrate (1) together with the projecting free carrier substrate islands (71) and mesa trenches (10) are then completely overformed by an auxiliary material (14), and

the singulation is carried out in accordance with method step (h) by applying a carrier film (15) over the electrical contacts (8) on the semiconductor layer (2) and selectively removing the auxiliary material (14).

47. (original) The method as claimed in claim 46, in which a metal, polymer and/or glass-based material is used as the auxiliary material (14).

48. (withdrawn) The method as claimed in claim 15, in which
the application of the adhesion and wetting layer (6) in accordance with method step (c) is restricted only to the surface of the outermost layer,

prior to method step (d), the mesa trenches (10) are completely covered with an anti-wetting layer (16),

the application of the carrier substrate (7) in accordance with method step (d) accordingly takes place only onto the adhesion and wetting layer (6) and is stopped before adjacent carrier substrate islands (71) grow together,

the entire structure above the growth substrate (1) together with the projecting free carrier substrate islands (71) and mesa trenches (10) are completely overformed by an auxiliary material (14), and

the singulation is carried out in accordance with method step (h) by applying a carrier

film (15) over the electrical contacts (8) on the semiconductor layer (2) and selectively removing the auxiliary material (14).

49. (withdrawn) The method as claimed in claim 15, in which the production or the deposition of the carrier substrate (7) onto the adhesion and wetting layer (6) in accordance with method step (d) is carried out in the following manner:

a photoresist is applied to the wetting layer (6) and patterned correspondingly throughout such that one or a plurality of negative forms of vertical structure elements (25) arise,

the carrier substrate is applied into the negative forms and onto the photoresist until the formation of a carrier base (24) above the photoresist.

50. (withdrawn) The method as claimed in claim 49, in which the photoresist is selectively removed.

51. (withdrawn) The method as claimed in claim 50, in which the interspaces (26) resulting from removal of the photoresist are filled with a filling material (27).

52. (withdrawn) The method as claimed in claim 51, in which a filling material (27) more elastic than the material of the carrier substrate (7) is used.

53. (withdrawn) The method as claimed in claim 49, in which the photoresist is patterned in such a way that at least one negative form of a vertical structure element is provided below the center of the semiconductor layer (2).